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843.38981CC4

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants: K. SUZUKI et al
Serial No.: 10/648,302
Filed: August 27, 2003
For: SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE
AND METHOD OF MANUFACTURING THE SAME
Group: 2815
Examiner: J. NGUYEN

RESPONSE TO ELECTION REQUIREMENT

Commissioner for Patents
POB 1450
Alexandria, VA 22313-1450

Sept. 13, 2004

Sir:

In reply to the outstanding Office Action, dated August 12, 2004, the following responsive remarks to the election requirement made are respectfully submitted in connection with the above-identified application.

The requirement made by the Examiner, namely, to elect a single disclosed species from that of Species I, Species II and Species III, as detailed on pages 2-3 of the Office Action, is noted. Accordingly, applicants, through their undersigned representative, provisionally elect Species III, in which the various example embodiments covered by Figs. 1-20 are related thereto, and request examination therefor of at least claims 19-26, which are readable thereon.

Notwithstanding the above election of Species III, applicants request that the remaining claims be examined, also, noting that they all include overlapping claimed subject matter. Regarding this, it is noted that independent claim 19 can be considered as generic to independent claim 15 of listed Species II. Using the example showings in Fig. 5, although not limited thereto, MISFET Qn4 or Qp4 relates to the "second MISFET" of claim 19 and, correspondingly, relates to the claimed "first MISFET" of independent claim 15. Further, the capacitive element shown in Fig. 5 of the drawings can be considered as one example showing relating to the "first capacitive element" according to claim 19 of the elected Species III as well as to the claimed "capacitive element" according to claim 15 of Species II. The thickness relationships of the gate insulating films associated with independent claim 15 are generically covered by those given in independent claim 19 of the elected Species III. With regard to this, independent claim 15 (of listed Species II) calls for both the "first MISFET" and for the "capacitive element" of the claimed semiconductor IC device to have a "first gate insulating film" which means, in effect, that the gate film thickness for both elements are the same. An example of this is shown by gate oxide film 9B with regard to the gate insulator associated with the capacitive element as well as that of MISFETs Qn4 or Qp4 in Fig. 5. Also, according to claim 15, the gate insulating film of the "second MISFET" (e.g., MISFET Qn1, Qp1) thereof has a smaller thickness than the "first gate insulating film," specifically, it has a thickness less than 3 nm. The corresponding gate insulator film relationships set forth in independent claim 19 (of listed Species III), it is noted, are consistent with these gate insulating film thickness relationships, although without requiring that both the "second

MISFET" and the "first capacitive element" in claim 19 have a same gate insulating film and a same gate electrode. The other featured aspects called for such as with regard to the "wherein" clauses of independent claim 15, it is noted, are contained in independent claim 19. The limiting aspects of the dependent claims 16-18 of listed Species II are likewise set forth in dependent claims 20-22, respectively.

A careful comparison between that of claims 19-26 (of listed Species III) and that of claims 1-14, corresponding to listed Species I, it is submitted, also shows that they contain a substantial amount of overlapping claimed subject matter. In fact, it is submitted, one can consider independent claim 23 as generically reading on each of claims 1+, 6+, 9+ and 12+ of listed Species I in the Office Action. Using the example embodiment of Fig. 5 of the drawings, for purposes of this showing, although not limited thereto, MISFET Qn1 or Qp1 relate to the claimed "first MISFET", MISFET Qn4 or Qp4 relate to the claimed "second MISFET" and the characteristic structure of the capacitive element shown in Fig. 5 relates to the "first capacitive element" of claim 23.

Correspondingly, the set forth first MISFET, second MISFET and first capacitive element in claims 1+, claims 6+, claim 9+ are thereby covered by the similarly named structural elements according to independent claim 23 (of listed Species III). That is, noting that independent claim 23 calls for a semiconductor integrated circuit device similarly to each of the independent claim groups related to listed Species I, although without the specifically set forth limiting language pertaining to the "third MISFET for a memory cell ... " of claims 1+, 6+, 9+ and 12+, it can be said that at least independent claim 23 of listed Species III is generic to the claims of listed Species I. Likewise, the set

forth second MISFET, the first MISFET and capacitive element according to independent claim 15 (of listed Species II) are covered by the set forth first MISFET, second MISFET and the first capacitive element of independent claim 23 (of listed Species III), respectively. Notwithstanding the differences existing therebetween, claim 23 (in addition to claim 19), it is submitted, is also generic to claims 15-18 of listed Species II. Accordingly, if as a result of examination of the present application, it is determined that at least claim 23 of listed Species III is allowable, examination of all of the claims of listed Species I and II, also, is respectfully requested.

Notwithstanding differences existing between the claims of different groupings, a common examination should nonetheless be given to all of the claims. This is because a significant commonality has been shown to be present between them. As a result, therefore, a substantial amount of overlapping would necessarily be effected in connection with the state-of-the-art searching between the claims of the different groupings. Accordingly, applicants, through their undersigned representative, respectfully urge the Examiner to include, also, claims 1-18 along with the claims 19-26 (directed to the provisionally elected Species III) for purposes of examination. According to U. S. practice and as set forth in MPEP 803:

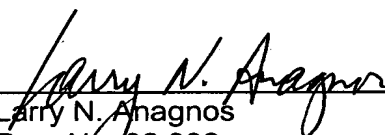
"[I]f the search and examination of an entire application can be made without serious burden, the Examiner must examine it on the merits, even though it includes claims to distinct or independent invention."

Therefore, for the reasons noted above, examination of all of the claims, i.e., claims 1-26, is respectfully requested. However, should the Election Requirement be maintained, examination of claims 19-26 and, moreover, also of claims 15-18 should be given in view of the above discussion. Should a

generic claim such as claim 23 become allowable, it is respectfully requested that examination be made of all claims that are readable on the non-elected species.

To the extent necessary, applicants petition for an extension of time under 37 CFR §1.136. Please charge any shortage in the fees due in connection with the filing of this paper, to the Deposit Account of Antonelli, Terry, Stout & Kraus, LLP, Dep. Acct. No. 01-2135 (843.38981CC4), and please credit any excess fees to such deposit account.

Respectfully submitted,
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